ABSTRACT

Metal-Oxide-Semiconductor–MOS devices presented here with thermally grown oxide layer of 3.04-5.92 nm thick were fabricated using p-type Si substrate. Capacitance-voltage (C-V) and conductance-voltage (G/ω-V) characteristics in frequency range of 10 kHz-100 kHz between 22 and 100 °C were measured in darkness. Current-voltage (I-V) was measured at T_room in darkness. C-V and G/ω-V at various frequencies revealed the energy distribution of MOS interface states. Current transport mechanisms in the device were studied and the I-V was generally characterised by Fowler-Nordheim and direct tunnel mechanisms of current carriers transport. Interface state density, flat-band voltages and frequency dispersion were extracted from C-V measurements. The frequency dispersion indicates the presence of either interface traps or laterally inhomogeneous distribution of defect centres near Si/SiO₂ interface. The concentration of charged defects and their location at Si/SiO₂ interface were calculated from frequency characterization. Small densities of interface traps < 2x10¹¹ eV⁻¹ cm⁻² show that SiO₂-Si interface has reliable qualities and its oxide may find applications in CMOS as dielectric gates. C-V of sample of dox = 4.14 nm was used to calculate at (22, 30, 50, 75, 100 °C) the capacitance in accumulation mode, interface charge density, flat band voltage, threshold voltage and density of interface traps (in minimum position), D_it = 0.3x10¹¹-1x10¹¹ cm⁻². G/ω-V characteristics at T_room for sample of dox = 4.14 nm at 10 kHz, 50 kHz and 100 kHz were obtained. C-V of all 4 samples at T_room was also used to calculate the mentioned oxide properties.
Two samples of $d_{ox}$ = 3.04 nm and 4.14 nm were studied using X-ray photoelectron spectroscopy technique and evaluation of Si 2p peak was obtained for $d_{ox}$ = 3.04 nm. Exact SiO$_2$ thickness for all samples was measured by an ellipsometer.

**Keywords:** Metal-oxide-semiconductor structures; ultrathin silicon dioxide layer; current-voltage characteristics; capacitance – voltage characteristics; conductance – voltage characteristics.

1. INTRODUCTION

The microelectronics industry, including internet and telecommunications revolutions, owes its success largely to the existence of thermal silicon dioxide. Circuits are made denser so that the SiO$_2$ layer thickness is 2 nm or less, and the reliability of such ultrathin oxide layers has become a major concern for continued scaling [1]. Silicon dioxide has unique properties due to its familiarity, versatility, and reliability i.e. stable in water and at elevated temperatures, an excellent electrical insulator, a mask to common diffusing species, and used to study properties of semiconductor-insulator interfaces [2-8]. Tunnel MOS device is a metal-oxide-semiconductor device, where the charge transfer is carried out by means of a direct tunnelling. In the last years this device is one of the most important objects of investigations in the field of technical semiconductor physics [8]. Direct tunnelling is known in MOS device with ultra-thin oxide (< 4 nm) during which electrons from the conduction band in a semiconductor are transferred across the oxide directly into the conduction band of metal with high probability [3,4]. Several investigations [8 – 14] made it clear that ultra-thin SiO$_2$ (1 – 3 nm) can be applied as a gate insulator in FET.

The MOS device is considered as an alternative to the p-n junction in the solar cell applications because of its simple and low cost fabrication process. The importance of the ultrathin oxide layer, in MOS device, lies in the passivation of silicon surface and the collection of photogenerated charge carriers by tunnelling effect [10]. Quality of the oxide layer can be improved by post oxidation annealing treatment [11]. The above stated information confirms the high importance of investigations of electrical-physical characteristics of MOS device with the ultrathin SiO$_2$ layer.

2. EXPERIMENTAL

Four p-Si wafers/substrates with (100) orientation and resistivity of 20 Ω·cm, 4 inch diameter with one polished surface, and of thickness ~ 380 μm were cleaned in sulfuric peroxide at 150°C for ~ 5 min. This procedure was followed by de-ionised water clean for 10 min (resistivity of the water was ≥ 10 MΩ). Then the wafers were etched by HF solution and followed by de-ionised water clean for 10 min.

Dry thermal oxidation, which has the best quality, at 800°C for 5 - 20 min, under a pure oxygen gas atmosphere, was obtained to form SiO$_2$ layer on silicon surface. The oxidation rate was low (< 100 nm/h) to control accurately the final oxide thickness. The exact thickness of SiO$_2$ layers was measured by an ellipsometer. A photoresist film was spun-coated on the front wafer surfaces followed by HF solution etching for the backside of wafers and then de-ionized water clean for 10 min. SiO$_2$ layers growth time and their thicknesses for 4 wafers are given in Table 1 and schematic diagram of the device is shown in Fig. 1. Top Al layer of 1 μm thick was sputtered using electron beam technique, in vacuum at $1 \times 10^{-6}$ torr. The sputtering was carried out through a mechanical mask so that circular electrodes of the diameter of 1600 μm were formed on top of the polished surface. Then back Al - metal layer of 1 μm thick was sputtered using e-beam, on the back side/unpolished surface.

The measurements of current-voltage (I-V) characteristics were carried out using Keithley 236 source measurement unit (Fig. 2):

- The measurements always took place in darkness;
- The measurements started at accumulation in the range from -3 V to +3 V.

<table>
<thead>
<tr>
<th>Al top electrode (1 μm thick)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$ Layer (3 - 6 nm)</td>
</tr>
<tr>
<td>p-Si substrate</td>
</tr>
<tr>
<td>20 Ohm.cm</td>
</tr>
<tr>
<td>380 μm thick- (100) orientation</td>
</tr>
<tr>
<td>Al bottom electrode (1 μm thick)</td>
</tr>
</tbody>
</table>

Fig. 1. Schematic diagram of the investigated MOS device
Table 1. SiO$_2$ layers growth time and their thicknesses for 4 wafers

<table>
<thead>
<tr>
<th>Sample #</th>
<th>SiO$_2$ growth time, min</th>
<th>SiO$_2$ thickness, nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>4.14</td>
</tr>
<tr>
<td>2</td>
<td>15</td>
<td>5.1</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>3.04</td>
</tr>
<tr>
<td>4</td>
<td>20</td>
<td>5.92</td>
</tr>
</tbody>
</table>

The measurements of capacitance-voltage (C-V) characteristics took place using HP 4284A Precision LCR Bridge setup (Fig. 3).

The measurements settings were as follows:

- The measurements always took place in darkness;
- The measurement frequencies were 10 kHz, 50 kHz, 100 kHz respectively;
- Voltage sweep -3 to 3 V and 3 to -3 V;
- Capacitance relaxation was measured after a voltage jump from -3 V to +3 V, and a logarithmic time scale was used (6 minutes).

Analyzing the composition of two MOS devices was studied using X-ray photoelectron spectroscopy technique. “Physical Electronics ESCA 5700” setup with a non-monochromated Al K$_\alpha$ X-ray source was used. The analysed area $\sim 0.5$ mm$^2$ and the upper contaminating layer was removed with Ar$^+$ ion bombardment at 4 kV. A calibration of reference samples with silicon oxide layer was about 1.2 nm/min.

3. RESULTS AND DISCUSSION

I-V curves for all samples were measured in the dark and results of sample #1 of $d_{\text{ox}} = 4.14$ nm and #3 of $d_{\text{ox}} = 3.04$ nm were typical characteristics of all devices and plotted as shown in Fig. 4.

As a general rule there is a difference, by several orders of magnitude, between the forward current and reverse one for the MOS devices of different SiO$_2$ thicknesses (see Fig. 4).

Minority charge carriers for p-Si dominate in the MOS devices and have naturally a large metal-semiconductor barrier as a result of the work functions difference between Al and p-type Si [15–18].

The following effects concerned with tunneling electrons transfer in Si band gap could take place for MOS of p-Si substrate:

(1) non-resonance electron tunnelling from Si for (tunnelling-transparent) barriers of the space-charge region in Si and dielectric [4];
(2) Resonant electron tunnelling from Si through the double barrier with switching size-quantized discrete levels of space-charge region in Si, being in a quantum well placed between these two barriers. Experiments [3] showed that resonant electron tunnelling was displayed by an appearance of a section of the rapid current rise as switching next quantum level to the current transfer process [3];

(3) resonant electron tunnelling from metal created the current peak as a coincidence of one level of a quantum well placed energetically lower than metal Fermi level with the edge of Si bulk valence band [3];

(4) electrons tunnel and enter the conduction band of Si accumulating a quantum well, could cause an increase of voltages corresponding to the appearance of resonances, does not change the qualitative picture of transport process [2].

All the observed I-V characteristics were generally characterised by an exponential law (as shown in Fig. 5) which can be related to the tunnel mechanism of current carriers transport [19]. For the case of the presented work tunnelling mechanism of non-resonance electron transfer from Si bulk to metal was observed (see Fig. 6) [15].

In the accumulation mode of holes at voltages from -5 V to -1.5 V the current for sample # 3 of $d_{ox} = 3.04$ nm is larger than that for sample # 1 of $d_{ox} = 4.14$ nm due to the higher electric field for thinner dielectric layer. For this voltage region currents behaviour is well approximated by the Fowler-Nordheim tunnelling mechanism for both samples [20,21]. For the reverse I-V curve “plateau effect” behaviour is observed i.e. M.A.Green, F.D.King and J.Shewchun [16] have explained this behaviour by considering the distribution of the external applied voltage between the oxide layer and the semiconductor when the semiconductor surface undergoes a transfer from accumulation to depletion mode.

In the depletion mode in the voltage region from -1.5 V to 0 V for device # 1 ($d_{ox} = 4.14$ nm) the Fowler-Nordheim tunnelling mechanism approximation takes place, while for the other sample # 3 ($d_{ox} = 3.04$ nm) the direct tunnelling approximation takes place. The direct tunnelling mechanism took place in MOS devices with thin gate oxide (less than 4 nm) and at low electric field, like that in this presented work. For the voltage range from -0.5 V to 1 V a bad agreement of approximated and experimental curves is observed. The forward characteristics sometimes demonstrate the step-like behaviour: at first the current is low, then its step-like behaviour is observed and thereafter the current increases as seen in Fig. 4 for sample # 3 ($d_{ox} = 3.04$ nm) from -1 V to 0 V. This can be related to the presence of surface states at Si-SiO$_2$ interface and a complicated conduction mechanism [22, 23].

At positive applied voltage samples # 1 & 3 have some differences in the shape of the current curves and presence of the “plateau effect” was observed (Figs. 4-6). This effect could be due to the presence of electrostatic acting interface states in the vicinity or below mid-gap of the semiconductor [24]. Figs. 5 and 6 demonstrate that the Fowler-Nordheim tunnelling mechanism has taken place here.
The I-V behaviour, for forward and reverse bias for samples # 2 ($d_{ox}=5.1 \text{ nm}$) & # 4 ($d_{ox}=5.92 \text{ nm}$) is characterised by Fowler-Nordheim tunnel conductance mechanism.

An accurate modelling of tunnelling current in modern ultra-thin oxide MOS devices cannot be accomplished by widely used Fowler-Nordheim model since it implies a metal as a gate and a triangular barrier [25]. These are obsolete conditions for a high tunnelling probability to occur due to ultra-thin oxides of less than 4 nm [20]. Quantisation effects of electrons and holes in inversion and accumulation modes, several tunnelling mechanisms besides conduction band electron tunnelling and a trapezoidal barrier play a fundamental role in conduction [20].

### 3.1 Measurements and Analysis of C-V Characteristics (Room Temperature) at different Frequencies

Figs. 7, 8 and 9 are typical C-V characteristics, at various frequencies in the range of 10 – 100 kHz and for voltages in the range of -3 V to 3 V, of the MOS capacitors of $d_{ox}=5.92 \text{ nm}$ (sample # 4), $d_{ox}=5.1 \text{ nm}$ (sample # 2), $d_{ox}=4.14 \text{ nm}$ (sample # 1) and $d_{ox}=3.04 \text{ nm}$ (sample #3). These characteristics have revealed the existence of accumulation and depletion regions for the C-V curves. The plots show the expected high frequency C-V curve in accordance with the p-type substrate theory. It was noted that no hysteresis has been observed on C-V curves of the studied structures; this indicates the low concentrations of charges and mobile ions in the oxide layer [22].

Moreover, for Figs. 7, 8 and 9 at voltages larger than 2 V the inversion mode is not observed, but for samples of # 4 and # 2 the inversion mode is observed at 50 kHz. At frequency of 10 kHz one could assume that the deep depletion mode is observed for the same samples. Measurements were not made at higher positive voltages to avoid device breakdown and it is possible that the inversion mode could be observed at higher bias. For the voltage range from -1.5 V to 3 V the depletion region presumably took place [4].

The normalised experimental C-V characteristics shift from the ideal one is present in the MOS devices due to non-ideal effects [4]. The 50 kHz or 10 kHz C-V plot measured at room temperature was shifted toward more negative voltages compared with the ideal C-V one. This shift has shown that there are fixed dielectric charge built-up in the SiO$_2$ film [4]. The related defects were positively charged, while the fixed oxide charge is always in SiO$_2$-Si interface/trap sites, spatially distributed farther from the Si-SiO$_2$ interface into the oxide.

<table>
<thead>
<tr>
<th>Sample #</th>
<th>SiO$<em>2$ film thickness, $d</em>{ox}$, nm</th>
<th>Oxide Cap. $C_{ox}$, nF (meas. Freq.)</th>
<th>Charge density at interface, $Q_{INT}$, C/cm$^2$</th>
<th>Flat band voltage, $V_{FB}$, V</th>
<th>Threshold voltage, $V_{TH}$</th>
<th>Density of interface traps, $D_{it}$, cm$^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>5.92</td>
<td>11.7 (f=50kHz)</td>
<td>$6.4 \times 10^8$</td>
<td>-0.74</td>
<td>-0.084</td>
<td>$1 \times 10^{11}$</td>
</tr>
<tr>
<td>2</td>
<td>5.1</td>
<td>13.5 (f=50kHz)</td>
<td>$5.8 \times 10^8$</td>
<td>-0.75</td>
<td>-0.042</td>
<td>$1.0 \times 10^{11}$</td>
</tr>
<tr>
<td>1</td>
<td>4.14</td>
<td>16.7 (f=10kHz)</td>
<td>$1.1 \times 10^7$</td>
<td>-0.57</td>
<td>-0.051</td>
<td>$0.6 \times 10^{11}$</td>
</tr>
<tr>
<td>3</td>
<td>3.04</td>
<td>22.7 (f=10 kHz)</td>
<td>$8.9 \times 10^6$</td>
<td>-0.66</td>
<td>-0.083</td>
<td>$0.6 \times 10^{11}$</td>
</tr>
</tbody>
</table>

*Fig. 7. Experimental C-V characteristics of MOS devices /p-type Si of oxide thickness $d_{ox}=5.92 \text{ nm}$ (sample # 4) (a) and 5.1 nm (sample #2) (b)*
The flat-band voltage ($V_{FB}$) obtained for each sample are related to the normalized capacitance curves [2,4]. The values of $V_{FB}$ are -0.74 V, -0.75 V, -0.57 V and -0.66 V for oxide thicknesses of 5.92 nm, 5.1 nm, 4.14 nm, and 3.04 nm respectively (Table 2).

Finally, the density of interface trap states ($D_{it}$) in the conduction band edge was calculated using the Terman method [27]. Figs. 9 b–10 b represent the density of interface trap state level as a function of energy in the region from 0.3 to 0.5 eV in the band gap of crystalline silicon. In
this region the minimum of $D_{it}$ versus $E_v$ shifts toward the middle of Si band gap with the decrease of SiO$_2$ film thickness from 5.92 to 3.04 nm. The average values of $D_{it}$ in this minimum is $0.6 \times 10^{11}$ cm$^{-2}$ (for $d_{ox} = 4.14$ nm and $d_{ox} = 3.04$ nm), $1.0 \times 10^{11}$ cm$^{-2}$ (for $d_{ox} = 5.1$ nm and $d_{ox} = 5.92$ nm).

The obtained data are in good agreement with the curves in Figs. 7, 8 and 9, i.e. the interface states follow the applied AC signal and result in excess capacitance which causes apparition of a peak at voltages ranging from 0 V to 2 V. Moreover, as the frequency increased the peak magnitude decreased as the interface states having difficulty to follow the AC signal, as a result of the slow surface states [23]. Therefore one can conclude that MOS samples with a dielectric thickness of 3 - 4 nm has an average surface state density of about $0.6 \times 10^{11}$ cm$^{-2}$, which is a good parameter for the tunnel MOS device.

3.2 Measurements and Analysis of G - V Characteristics at Different Frequencies

Typical conductance $G/\omega$-V plots measured at frequencies of 10 – 100 kHz for MOS device # 1 are shown in Fig. 11 [28].

![Fig. 11. Experimental G/ω - V characteristics of MOS device # 1 of oxide thickness $d_{ox}$ = 4.14 nm at frequencies of 10 – 100 kHz /p-type Si](image)

For frequencies of 50 kHz and 100 kHz, the $G/\omega$ -V curves have coincided with each other in the accumulation mode and the conductance is independent on the applied bias. Therefore, the saturation of the high frequency conductance in accumulation mode indicates that the ratio of the leakage carriers is small compared to the total carriers as observed in ordinary MOS capacitor [28,29]. For the 10 kHz frequency, the measured signal $G/\omega$ has increased as the voltage increased indicating the presence of leakage current through the oxide layer which contains traps allowing carriers to leak through it. The conductance in accumulation mode was determined by the concentrated positive charge carriers caused by the structure functioning mode and the embedded positive oxide charge [26].

As the negative electric field decreases in the region from - 1.5 to - 0.5 V (the depletion mode) one observes a reduction of conductance value. The $G/\omega$ - V curves show a minimum in the voltage region of - 0.5 to 0 V. Moreover, as the frequency increased position of the minimum shifted towards the positive voltage region. All these characteristics and features confirm the assumption that the deep trap levels being present in the bulk of the SiO$_2$ film and slow traps at the SiO$_2$-Si interface took part in the conduction process [30].

After changing the voltage polarity (now positive voltage), positive part of the conductance start decreasing for 50 kHz and 100 kHz as a result of recombination processes but for the 10 kHz a contrary situation was observed Fig.11. The increase of total conductance could be related to a larger contribution of the conductance component connected with the slow trap states at the SiO$_2$-Si interface [30].

3.3 Measurements and analysis of C-V and G-V Characteristics at Different Temperatures

The C-V characteristics of sample # 1 ($d_{ox} = 4.14$ nm) at different temperatures (22-100 °C) and at 100 kHz frequency are shown in Fig. 12. Small changes of the C-V characteristics and the flat bands stress were observed as temperature changes. This is related to the Fermi level movement relative to the surface states [31, 32]. Calculations of the capacitance-voltage characteristics of MOS device as a function of measured temperature are presented in Table 3. The temperature dependence measurements, and for a wide temperature range, have shown that the average values of $D_{it}$ are in the order of $1 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ (Fig. 13).
Table 3. C-V Calculations of MOS-device as a function of measured temperature for sample # 1 of dox = 4.14 nm. [26]

<table>
<thead>
<tr>
<th>Status</th>
<th>Temperatures, °C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>22</td>
</tr>
<tr>
<td>Device Capacitance in accumulation mode, nF</td>
<td>3.86</td>
</tr>
<tr>
<td>Charge density at the interface, C/cm²</td>
<td>1.3 × 10⁻⁷</td>
</tr>
<tr>
<td>Flat band voltage, V FB</td>
<td>-0.49</td>
</tr>
<tr>
<td>Threshold voltage, V</td>
<td>-0.033</td>
</tr>
<tr>
<td>Density of interface traps</td>
<td>0.9× 10⁻¹⁰</td>
</tr>
</tbody>
</table>

Table 3 indicated that the threshold voltage has considerably changed at 50°C. One of the reasons of instability of MOS charge properties is the migration of mobile ions in the dielectric layer. This ions migration was carried out through the oxide film and along the interface and led to the existence of the immobile charges. Excessive silicon atoms and other impurities could be the main source of induced charge in SiO₂ [4].

The measured conductivity G-V data for sample # 1 (dox = 4.14 nm) at different temperatures and at 100 kHz frequency are shown in Fig.14. The conductivity increased insignificantly as temperature increased and that is the characteristic property of the semiconductors and dielectrics [4]. The increase of temperature led to the increase of minority carrier generation rate and the probability of charges emission in the allowed band by surface states. The work of [33] considered two temperature-dependent mechanisms of minority carriers: (1) thermal generation of the carriers with the participation of generation-recombination centres in the band gap; (2) generation of minority carriers through centres in the silicon oxide. The generation of minority carriers through traps in the oxide layer is different from that generation on the surface centres/volume and characterised by strong dependence on the field in silicon oxide [33].

3.4 XPS Measurements Results

The XPS investigations of 2 samples # 3 & # 1 with silicon oxide thickness of 3.04 nm and 4.14 nm respectively were carried out. The XPS
Fig. 15. XPS spectrum of sample # 3 of $d_{ox}=3.04$ nm

spectrum in Fig. 15 shows the surface of sample # 3 after Ar ion bombardment (removal of approximately 1 nm) depending on binding energy. XPS confirmed the oxide thickness of 3.04 nm for the mentioned sample, due to the evaluation of the Si 2p peaks.

4. CONCLUSIONS

Al/SiO$_2$/Si devices presented here with thermally grown oxide layer of 3.04 - 5.92 nm thick were fabricated using p-type Si substrate. C-V and G$/\omega$-V characteristics in the frequency range of 10 kHz - 100 kHz at temperatures between 22 and 100 °C were measured in the dark. I-V characteristics of the devices were measured at room temperature and in the dark. The C-V and G$/\omega$-V measurements at various frequencies gave important information about the energy distribution of the interface states of the MOS device. The current transport mechanisms in the device were studied, the I-V characteristics were generally characterised by the Fowler - Nordheim and direct tunnel mechanisms of current carriers transport. Interface state density, flat-band voltages and the frequency dispersion were extracted from the C-V measurements (experimental data). The frequency dispersion properties reveal the presence of either interface traps or a laterally inhomogeneous distribution of defect centres within the oxide near the interface Si/SiO$_2$. The concentration of charged defects and their location in the Si/SiO$_2$ interface region were calculated from frequency characterisation. The relatively small densities of interface traps ($<2 \times 10^{11}$ eV$^{-1}$cm$^{-2}$) indicate that SiO$_2$-Si interface has a reliable quality and its oxide may find applications in the CMOS as a gate dielectric.

Two samples of oxide thickness of 3.04 nm and 4.14 nm were studied using X-ray photoelectron spectroscopy technique and the evaluation of the Si 2p peak led to an oxide thickness of 3.04 nm for sample #3. The exact thickness of SiO$_2$ layers for all samples was measured by an ellipsometer.

C-V measurements of sample #1 of $d_{ox}=4.14$ nm was used to calculate at various temperatures (22, 30, 50, 75, 100°C) the capacitance in the accumulation mode, charge density at the interface, flat band voltage, threshold voltage and density of interface traps (in minimum position), $D_{it}$, cm$^{-2}$ ($D_{it}=0.3 \times 10^{11}$-$1 \times 10^{12}$ cm$^{-2}$). G$/\omega$ - V characteristics at room temperature for sample #1 ($d_{ox}=4.14$ nm) and at 10 kHz, 50 kHz and 100 kHz were obtained.

C-V measurements of all samples # 1 - # 4 at room temperature were also used to calculate the mentioned oxide properties.
It was found that both of the capacitance and conductance were quite sensitive to frequency, in the accumulation region as the frequency increased the plateau values \( C/C_{ox} \) decreased, corresponding to the oxide capacitance and conductivity values. That was explained by the presence of series resistance, \( R_s \), i.e. about 40 Ohm for samples \# 4 and \# 2 measured at 50 kHz; but for samples \# 1 and \# 3 at 10 kHz, and \( R_s \) value decreased at higher frequencies.

The values of \( V_{FB} \) are - 0.74 V, - 0.75 V, - 0.57 V and - 0.66 V for oxide thicknesses of 5.92 nm, 5.1 nm, 4.14 nm, and 3.04 nm respectively. The density of interface trap states (\( D_{it} \)) for MOS capacitors in the conduction band edge were found to be \( 0.6 \times 10^{11} \text{ cm}^{-2} \text{eV}^{-1} \) (for \( d_{ox} = 4.14 \text{ nm} \) and \( d_{ox} = 3.04 \text{ nm} \)), \( 1.0 \times 10^{11} \text{ cm}^{-2} \text{eV}^{-1} \) (for \( d_{ox} = 5.1 \text{ nm} \) and \( d_{ox} = 5.92 \text{ nm} \)). i.e. very small variations.

The behaviour of C-V and \( G/\omega -V \) dependences on temperature can be related to surface states in the \( \text{SiO}_2\text{-Si} \) interface region. The temperature dependence measurements have shown that for a wide temperature range, the average values of \( D_{it} \) are in the order of \( 1 \times 10^{11} \text{ cm}^{-2} \text{eV}^{-1} \).

The interface states and the interfacial insulator layer at the metal/semiconductor interface play an important role in the determination of the characteristics parameters of the devices, which are responsible for the non-ideal behaviour of I-V, C-V and \( G/\omega -V \) characteristics. Experimental results show that both \( D_{it} \) and \( R_s \) are important parameters influence the electrical characteristics of the MOS device.

The XPS investigations of 2 samples \# 3 & \# 1 with silicon oxide thickness of 3.04 nm and 4.14 nm respectively, after \( \text{Ar}^+ \) ion bombardment (with a layer removal of approximately 1 nm) have confirmed the oxide thickness magnitudes, due to the evaluation of the Si \( 2p \) peaks.

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**COMPETING INTERESTS**

Author has declared that no competing interests exist.

**REFERENCES**


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